CSE 502: Computer Architecture

Instruction Commit
The End of the Road (um... Pipe)

- Commit is typically the last stage of the pipeline
- Anything an insn. does at this point is *irrevocable*
  - Only actions following sequential execution allowed
  - E.g., wrong path instructions may not commit
    - They do not exist in the sequential execution
Everything Should Appear In-Order

- ISA defines program execution in sequential order
- To the outside, CPU must appear to execute in order
“Looking” at CPU State

• When OS swaps contexts
  – OS saves the current program state (requires “looking”)
  – Allows restoring the state later

• When program has a fault (e.g., page fault)
  – OS steps in and “looks” at the “current” CPU state
Implementation in the CPU

• ARF keeps state corresponding to committed insns.
  – Commit from ROB happens in order
  – ARF always contains some RF state of sequential execution

• Whoever wants to “look” should look in ARF
  – What about insns. that executed out of order?
Only the Sequential Part Matters

Sequential View of the Processor

State of the Superscalar Out-of-Order Processor

What if there’s no ARF?
If you need to “see” a register, you go through the aRAT first.
Wrong-path instructions are flushed…
architected state has never been touched

Fetch correct path instructions
Which can update the architected state when they commit
Committing Instructions (1/2)

- “Retire” vs. “Commit”
  - Sometimes people use this to mean the same thing
  - Sometimes they mean different things
    - Check the context!

- Insn. *commits* by making “effects” visible
  - (A)RF, Memory/$, PC
Committed Instructions (2/2)

- When an insn. executes, it modifies processor state
  - Update a register
  - Update memory
  - Update the PC

- To make “effects” visible, core copies values
  - Value from Physical Reg to Architected Reg
  - Value from LSQ to memory/cache
  - Value from ROB to Architected PC
Blocked Commit

• To commit $N$ insns. per cycle, ROB needs $N$ ports
  – (in *addition to* ports for dispatch, issue, exec, and WB)

Can’t reuse ROB entries until all in block have committed. Can’t commit across blocks.

Reduces cost, lowers IPC due to constraints.
Faults

• Divide-by-Zero, Overflow, Page-Fault
• All occur at a specific point in execution (precise)

CPU maintains appearance of sequential execution
Timing of DBZ Fault

• Need to hold on to your faults

On a fault, flush the machine and switch to the kernel

Let earlier instructions commit
The arch. state is the same as just before the divide executed in the sequential order
Now, raise the DBZ fault and when you switch to the kernel, everything appears as it should

Just make note of the fault, but don’t do anything (yet)
Speculative Faults

- Faults might not be faults...

Which is what we want, since in a sequential execution, the wrong-path divide would not have executed (and faulted)

Buffer faults until commit to avoid speculative faults
Timing of TLB Miss

- Store must re-execute (or re-commit)
  - Cannot leave the ROB

Store TLB miss can stall the core
Load Faults are Similar

• Load issues, misses in TLB
  – When load is oldest, switch to kernel for page-table walk
    ...could be painful; there are lots of loads

• Modern processors use hardware page-table walkers
  – OS loads a few registers with PT information (pointers)
  – Simple logic fetches mapping info from memory
  – Requires page-table format is specified by the ISA
Asynchronous Interrupts

• Some interrupts are not associated with insns.
  – Timer interrupt
  – I/O interrupt (disk, network, etc...)
  – Low battery, UPS shutdown

• When the CPU “notices” doesn’t matter (too much)
Two Options for Handling Async Interrupts

• Handle immediately
  – Use current architected state and flush the pipeline

• Deferred
  – Stop fetching, let processor drain, then switch to handler
    • What if CPU takes a fault in the mean time?
    • Which came “first”, the async. interrupt or the fault?
Store Retirement (1/2)

• Stores forward to later loads (for same address)
  – Normally, LSQ provides this facility

At commit, store
Updates cache

After store has left
the LSQ, the D$ can provide the correct value
Store Retirement (2/2)

• Can’t free LSQ Store entry until write is done
  – Enables forwarding until loads can get value from cache

• Have to re-check TLB when doing write
  – TLB contents at Execute were speculative

• Store may stall commit for a long time
  – If there’s a cache miss
  – If there’s a TLB miss (with HW TLB walk)

Don’t we check DTLB during store-address computation anyway? Do we need to do it again here?

All instructions may have successfully executed, but none can commit!
Writeback Buffer (1/2)

- Want to get stores out of the way quickly

Even if store misses in cache, entering WB buffer counts as committing.

- Allows other insns. to commit.

WB buffer is part of the cache hierarchy. May need to provide values to later loads.

- Cache can now provide the correct value.

Eventually, the cache update occurs, the WB buffer entry is emptied.

Usually fast, but potential structural hazard
Writeback Buffer (2/2)

- Stores enter WB Buffer in program order
- Multiple stores can exist to same address
  - Only the last store is “visible”

<table>
<thead>
<tr>
<th>Addr</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>42</td>
<td>1234</td>
</tr>
<tr>
<td>13</td>
<td>-1</td>
</tr>
<tr>
<td>8</td>
<td>90901</td>
</tr>
<tr>
<td>42</td>
<td>5678</td>
</tr>
</tbody>
</table>

No one can “see” this store anymore!
Write Combining Buffer (1/2)

- Augment WBB to combine writes together

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</table>

If Stores to same address, combine the writes
Write Combining Buffer (2/2)

- Can combine stores to same cache line

<table>
<thead>
<tr>
<th>$-Line Addr</th>
<th>Cache Line Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>80</td>
<td>1234</td>
</tr>
<tr>
<td></td>
<td>5678</td>
</tr>
</tbody>
</table>

One cache write can serve multiple original store instructions.

- Aggressiveness of write-combining may be limited by memory ordering model.
- Benefit: reduces cache traffic, reduces pressure on store buffers.
- Writeback/combining buffer can be implemented in/integrated with the MSHRs.
- Only certain memory regions may be "write-combinable" (e.g., USWC in x86).
Senior Store Queue

- Use STQ as WBB (not necessarily write combining)

While stores are completing, other accesses (loads, etc…) can continue getting the values from the “senior” STQ

New stores cannot allocate into Senior STQ entries until stores complete

No WBB and no stall on Store commit
Retire

- Insn. **retires** by cleaning up all related state
- Besides updating architected state
  ... needs to deallocate resources
  - ROB/LSQ entries
  - Physical register
  - “colors” of various sorts
  - RAT checkpoints
- Most are FIFO’s or Queues
  - Alloc/dealloc is usually just inc/dec head/tail pointers
- Unified PRF requires a little more work
  - Have to return “old” mapping to free list