Introduction

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CSE 502 - CompArch

- Computer Architecture is
  … the ***science*** and ***art*** of selecting (or designing) and interconnecting hardware and software components to ***create computers*** …
- Computer Architecture is an umbrella term
  - *Instruction Set Architecture (ISA)*: software-visible interface
  - *Micro-architecture*: internal organization of components
- This course is mostly about ***micro-architecture***
  - What's inside the processor (CPU)
  - What implications this has on software

CSE 502 - CompArch

- This course is roughly like CSE 506
  - In CSE 506, you learn what's inside an OS
  - In CSE 502, you learn what's inside a CPU
- This is a project-intensive course
  - Learn why things are the way they are, first hand
  - We will "build" emulators of CPU components

Why Study CompArch (1/3)

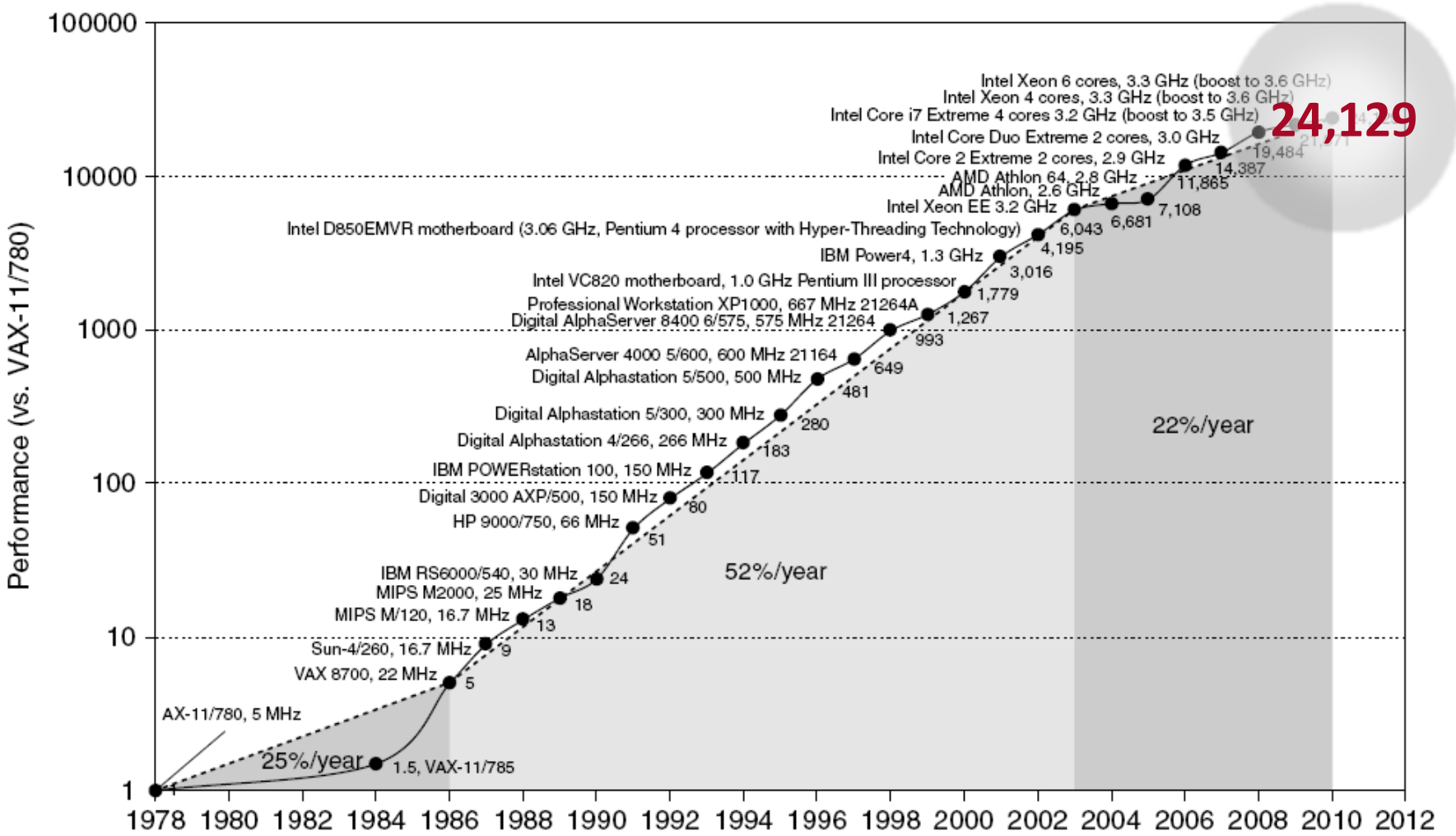
- You need one more qualifier/graduation requirement

✗ ***Bad answer!***

- You want to become a computer architect
- You want to learn what's inside a processor
  - Because you're curios (and there is no computer w/o a processor)
  - To write better/faster application code
  - To write system software (OS, compiler, etc.)
- Computer architecture is cool and intellectually fascinating
  - BTW, what is the most complex man-made device?
  - Hint: there are billions of individually designed and verified transistors in a modern processor chip

✓ ***More like it!***

Why Study CompArch (2/3)



Why Study CompArch (3/3)

Sources of performance improvement:

- Improvements in semi-conductor technology
  - Faster transistors
  - More transistors
- Improvements in computer architecture
  - *Computer architects work to turn the additional resources into speed/power savings/functionality!*

In this class, we will study some of the cool techniques invented by computer architects to make this possible!

Moore's Law

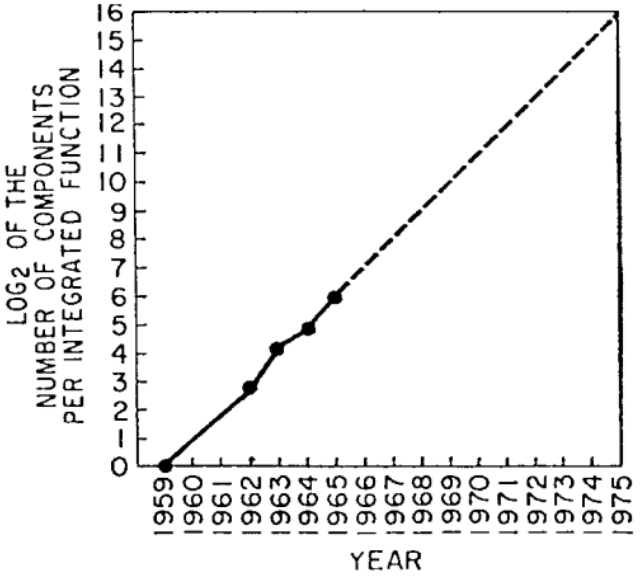
- 1st Moore's Law (1965)

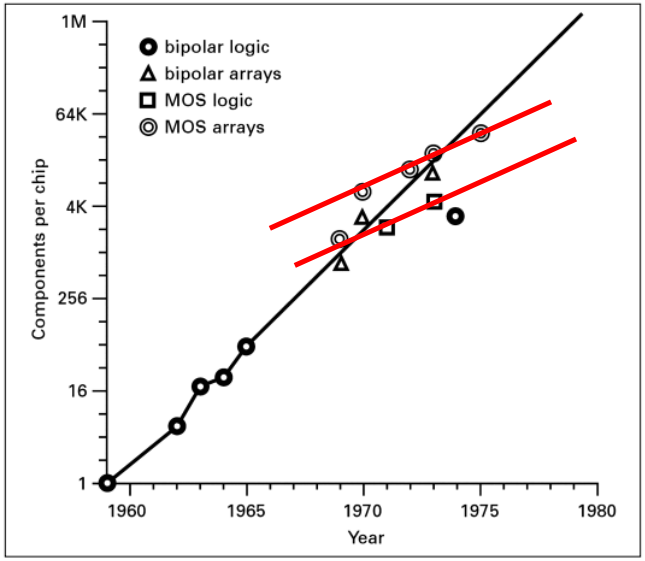
  "The complexity for minimum component costs has increased at a rate of roughly a factor of two per year. Certainly over the short term this rate can be expected to continue, if not to increase."

- 2nd Moore's Law (1975)

  "The new slope might approximate a doubling every two years, rather than every year"

- Nowadays, Moore's law is a general term for any exponential change in technology (with different slopes)
  - E.g., transistor size, transistor speed, processor performance, etc.

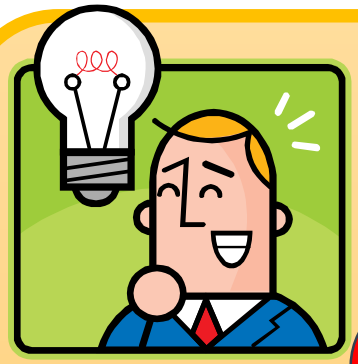




Course Topics

- Instruction Decode
- Pipelining
- ***Processor Front-end***
- ***Execution Core***
- ***Memory Hierarchy***
- Multi-socket, Multi-thread, Multi-core
- Vector Processing and GPUs, Data centers, …
  - Time permitting

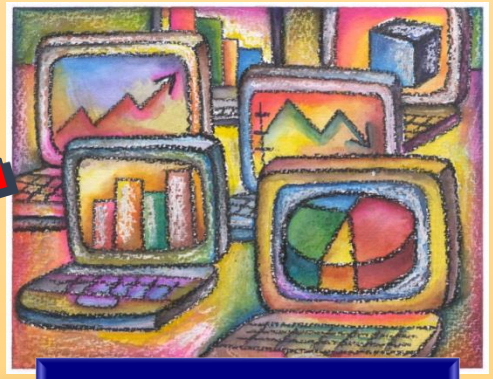
Hardware Design Process



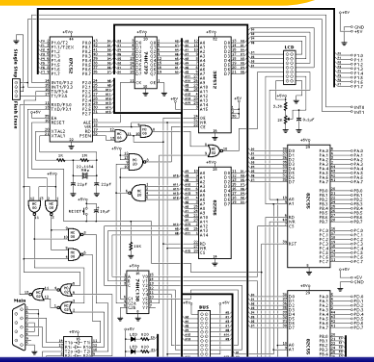
Conceptual Design

Behavioral Implementation

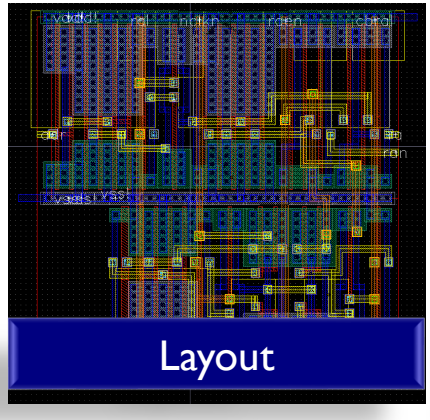
CSE 502



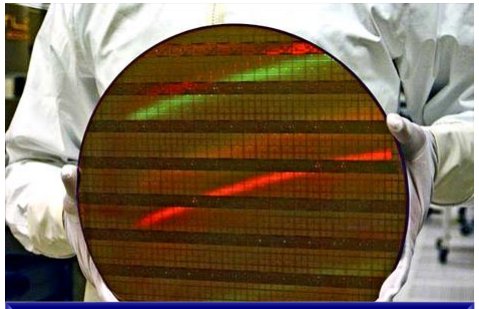
Evaluation



Structural Implementation



Layout



Manufacturing

Packaging

Grading

What?	Points
1 Quiz	0
2 Homeworks	10 each
Course Project	Up to 115
Midterm	15
Final	25
Participation	10
Total	**185**

Course Project	Points
5-Stage pipeline + direct-mapped caches	40
5-Stage pipeline + set-associative caches	45
Above + super-scalar pipeline	60
Above + out-of-order execution	80
Multi-cycle divider and pipelined multiplier on top of any of the above	5 extra
Branch prediction and speculative execution on top of any of the above	10 extra
SMT on top of any of the above	10 extra
Successful synthesis to FPGA on top of any of the above	10 extra

- Guaranteed grades: [A, A-, B+, …] = [95, 90, 85, …]
  - I may use a curve on top of this if need be

Course Project

- Goal: design and implement a SPARCv8 processor
  - Preferably a super-scalar, out-of-order one ☺
- We'll use SystemVerilog HDL for implementation
  - Don't panic! We'll cover the necessary background
  - Hopefully, will help you think and design like a HW designer
- I'll provide a cross-compiler and a simulation environment
  - You'll design and implement the processor
  - See course webpage for details

Logistics (1/3)

- Books
  - Recommended for reference, not required
    - I highly recommend reading both books cover-to-cover if you are targeting systems research
  - *Modern Processor Design: Fundamentals of Superscalar Processors*
  - *Computer Architecture: A Quantitative Approach* (H&P)
- There will be other required readings
  - SPARC Architecture Manual
  - SystemVerilog tutorials
  - And a few papers

Logistics (2/3)

- Working in groups: only permitted on the project
  - Groups may be up to ***2 people***
  - Should let me know of your groups by ***Feb 18***
- Attendance
  - Optional but affects your participation grade
  - No laptop, tablet, or phone use in class
    - Seriously! I ***will deduct*** grade points

Logistics (3/3)

- Blackboard
  - Grades will be posted there, nothing else
- Course forum and newsgroup
  - Subscription Is ***required***
  - **http://piazza.com/stonybrook/spring2016/cse502/home**
- Quiz
  - Completion is ***required***
  - If you missed the 1st class, come to office hours for it

Academic Integrity Policy

- You may...
  - Discuss assignment, design, techniques
- You may ***not***…
  - Share code
  - Use any code not distributed as part of project handouts
    - Exceptions are possible, but must receive explicit permission
  - If caught, you'll fail. No exceptions!

QUIZ