Shenghsun Cho

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EDUCATION

Stony Brook University, New York, U.S.A. Aug.2013 – Present
Ph.D. student in Computer Science, COMPAS Lab
- research in computer architecture, accelerators and operating systems

National Taiwan University, Taipei, Taiwan Sep.2005 – Jun.2007
M.S. in Electrical Engineering, High-Performance Computing Lab, GPA 4.0/4.0
- thesis in network packet classification architecture

National Central University, Chung-Li, Taiwan Sep.2000 – Jun.2005
B.S. in Computer Science and Information Engineering, Major GPA 3.57/4.0
- focus on embedded systems and mobile device programming

RESEARCH PROJECTS

Skip List Accelerator (SBU) Dec.2015– Present
- Design accelerator for offloading the skip list traversal of Google LevelDB
- Achieve shared virtual memory space between host and accelerator

Network Processor (SBU) Jun.2014– Present
- Save power by offloading TCP/IP while retaining full stack functionality
- Partition Linux TCP/IP stack across heterogeneous multi-core system

Host-Accelerator Communication (SBU) Jun.2014– Present
- Design fast and easy-to-use programming interfaces between host and accelerator
- MMU development for PCIe based accelerators
- Function call orchestration between cores with different ISAs

K-Nearest-Neighbors Accelerator using FPGA (SBU) Dec.2013 – May.2014
- Design multi-core KNN system on FPGA
- Achieve same performance as fast CPUs with much lower power consumption

Transactor between Virtual Platform and Physical Circuit (GUC) Oct.2007 – Oct.2010
- Link the virtual platform and the physical FPGA circuit as a single SoC
- RTL design, FPGA digital circuit, Linux kernel module and application development
- Convert SystemC TLM transactions to/from ARM AHB signals

Network Packet Classification Architecture (NTU) Feb.2006 – Jun.2007
- Architecture for packet classification with low and bounded memory consumption
- C++ model and FPGA digital circuit development
- Issued as U.S. Patent No. 7,953,082

COURSE PROJECTS

Computer Architecture: x86-64 Core (SBU) Feb.2014 – Jun.2014

- x86-64 ISA subset core design from scratch using SystemVerilog
- Design and implement micro-ops, super-scalar pipeline and set-associative cache

Operating Systems: SBUnix (SBU) Sep.2013 – Dec.2013

- x86-64 based Unix-like kernel design from scratch
- Design and implement virtual memory, process management and file system

WORK EXPERIENCE

Microsoft Research, Redmond, U.S.A Jun.2015 – Aug.2015
Intern, The Catapult Project

FPGA Circuit Design for Data Centers

- Algorithm implementation with high-level synthesis
- Multi-FPGA communication

Global Unichip Corp., Hsinchu, Taiwan (subsidiary of TSMC) Oct.2007 – Jun.2013
Senior Engineer, High Speed Interface IP Department

ASIC Tape-out

- LVDS 65nm/40nm customer ASIC tape-out
- V-By-One HS test chip tape-out

USB IP Design and Verification

- USB 3.0 PHY verification
- USB 2.0 MAC IP and PLI model development

LVDS/V-By-One HS IP Design

- 720MHz LVDS digital IP design
- Multiple wire skew control within picosecond level
- V-By-One HS digital IP design

Digital IP and Embedded Software Design

- AHB to AHB bridge digital IP design
- NAND Flash Linux driver for ARM platform development
- ARM platform standalone software development
- SystemC virtual IP with TLM interface development

SKILLS

Programming Languages: C/C++, x86 assembly
Hardware Design Languages: Verilog, SystemVerilog
Digital Design: RTL implementation, simulation, synthesis, FPGA
Digital Design Tools: VCS, Verdi, Quartus, ISE, Vivado, Synplify