Tianchu **Ji**

tianchu.ji@stonybrook.edu | chickenjohn | tianchu-ji

Education

Stony Brook University — *Stony Brook, NY*

PH.D. CANDIDATE, COMPUTER ENGINEERING — *Sept. 2016 - Present*

Huazhong University of Science and Technology — *Wuhan, China*

B.E., IC DESIGN AND INTEGRATED SYSTEMS — *Sept. 2012 - June 2016*

Research Projects

Long Short-Term Memory Neural Network Acceleration on FPGA — *Stony Brook, NY*

AHGO LAB AND COMPAS LAB@STONY BROOK UNIVERSITY — *Aug. 2018 - May 2020*

- Implement a highly scalable and resource-efficient FPGA hardware acceleration on FPGA
- Implement a cycle-accurate latency analyzer helping analyzing delay of LSTM computation
- Implement a Python optimizer which generates the optimized accelerator
- The accelerator requires less resource than existing design while still being able not to increase the latency

High Resolution Time-to-Digital Converter on FPGA — *Stony Brook, NY*

AHGO LAB AND COMPAS LAB@STONY BROOK UNIVERSITY — *May 2019 - April 2020*

- implement a high resolution Time-to-Digital Converter by making use of the dedicated carry chain blocks on Ultrascale+ FPGAs.

Deep Learning on Spectrum Sensing and its FPGA applications — *Stony Brook, NY*

AHGO LAB@STONY BROOK UNIVERSITY — *July 2018 - Sept. 2019*

- Deep Learning algorithms are found to have good performance on Spectrum Sensing tasks
- Evaluate the throughput latency of Tensorflow-based Deep Learning algorithms on CPU/GPU of both desktop and embedded device
- Investigate implementing Deep Learning accelerators on FPGA to cope with aforementioned tasks in real-time.

Scalable memory interconnect for many-port DNN accelerators on FPGA — *Stony Brook, NY*

AHGO LAB AND COMPAS LAB@STONY BROOK UNIVERSITY — *Jan. 2017 - July 2018*

- An interconnect is implemented between DNN accelerator and DRAM controller with wide data width without unnecessary flexibility
- Our design can both be scalable and reach high throughput.
- Our design reduces LUT and FF use by 4.7x and 6.0x, and improves frequency by 1.8x.

Working Experience

Amazon Web Services (AWS) Redshift AQUA Team — *East Palo Alto, CA*

SDE INTERN — *May. 2020 - Aug. 2020*

- Disabling DDR auto-refresh to improve the throughput
- Offline DDR Retention Time profiling and online DDR access checking
- DDR throughput improves by 1.29x

Skills

PROGRAMMING LANGUAGE

- Programming: C/C++, Python
- Hardware Description: Verilog, SystemVerilog, SpinalHDL
- High Level HDL: experience with Chisel
- Deep Learning Framework: Tensorflow

FPGA

- Xilinx FPGA: Spartan-6, Virtex-7 and Virtex-Ultrascale+

Publications

- Y.Shen, **T. Ji**, M. Ferdman, and P. Milder, "A scalable memory interconnect for many- port DNN accelerators and wide DRAM controller interfaces", in *28th International Conference on Field Programmable Logic and Applications(FPL).* IEEE, 2018.
- Y.Shen, **T. Ji**, M. Ferdman, and P. Milder, "Argus: an End-to-End Framework for Accelerating CNNs on FPGAs", in *IEEE Micro*, 2019.