Varun Agrawal

Ph.D. Candidate
COMPAS Lab
Stony Brook University

http://compas.cs.stonybrook.edu/~vagrawal/
vagrawal@cs.stonybrook.edu

Research Interests

Design fast and efficient computer systems. Particularly I'm interested in the design of processor microarchitecture, and studying the properties of applications and their interaction with the underlying hardware.

Education

- **Stony Brook University**, Stony Brook, NY. **August 2012 - Present**
  Ph.D. Candidate - Advised by Michael Ferdman, Department of Computer Science
  GPA: 3.91
- **Indian Institute of Technology Kanpur**, Kanpur, India. **July 2006 - May 2010**
  B.Tech., Electrical Engineering
  CPI: 8.3/10.0

Work Experience

- **Intern, Advanced Micro Devices**, Boxborough, MA, USA. **September 2017 - December 2017**
  - Improved efficiency of processor frontend in AMD's general purpose processors
- **Intern, Intel Corporation**, Hillsboro, OR, USA. **June 2015 - August 2015**
  - Code Generation for PCU microcontroller
- **Software Associate, Strand Life Sciences**, Bangalore, India. **August 2010 - June 2012**
  - Develop bioinformatics tools for gene expression analysis

Publications

Conference Publication

- **Architectural Support for Dynamic Linking** **ASPLOS 2015**
  Varun Agrawal, Abhiroop Dabral, Tapti Palit, Yongming Shen, Michael Ferdman, in 20th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2015.

Conference Poster

- **JIT Kernels: An Idea Whose Time Has (Just) Come** **SOSP 2013**
  Varun Agrawal, Amit Arya, Michael Ferdman, Donald E. Porter, Poster presented at the 24th ACM Symposium on Operating Systems Principles (SOSP poster), 2013.

Research Projects

- **Elider**
  - Predicting repeating instructions with identical inputs in applications
  - Implement hardware techniques to prevent redundant execution
- **MPSP**
  - Design a massively parallel server processor for high throughput servers
  - Re-think hardware and software interaction leveraging the similarity in request processing
- **Graph Algorithm Optimization**

  - Improve graph algorithm performance by reducing LLC misses
  - Improved data structure to store graph nodes

- **JIT Kernels**
  - JIT compile OS kernels to boot hardware optimized kernels.

Course Projects

- **Computer Architecture** **Spring 2013**
  - Designed superscalar out-of-order processor for a reduced x86 instruction set.
  - Speculative execution with a simple branch predictor.
- **Compiler Design** **Spring 2013**
  - Made a compiler for a simple object-oriented programming language, Proto.
- **Operating Systems** **Fall 2012**
  - Implemented critical portions of JOS operating system: bootloader, page tables, fork, and syscalls.
  - Implemented FUSE based filesystem with Git (version control) as backend.

Teaching Assistant

- **Computer Architecture (Graduate)**
  Instructor: Michael Ferdman **Spring 2014**
  Instructor: Nima Honarmand **Spring 2015**
- **Data Structures (Undergraduate)** **Fall 2012, Spring 2013**
  Instructor: Ahmad Esmaili

Technical Skills

Programming Languages C, C++, Java, Python, R, Shell script, SystemC

Softwares Condor, Intel Pin, Intel VTune, Simics

Professional Memberships

- Student Member of ACM SIGARCH & SIGOPS
- Student Member of IEEE Computer Society